

RAiO

RA6963

**Dot Matrix
LCD Controller
Specification**

Version 1.4

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RAiO Technology Inc.

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1. Overview

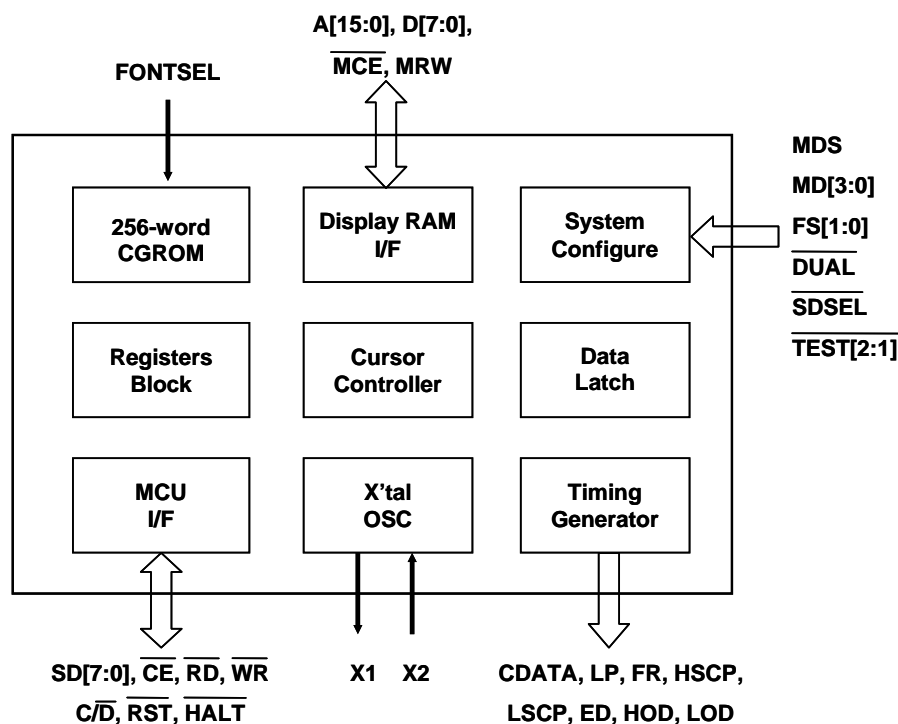
The RA6963 is a dot matrix LCD Controller which fully compatible with T6963C. It supports various LCD Driver for standard or custom-made LCD module. The RA6963 built-in a 256-word CG(Character Generator) ROM that for ASCII, Japanese and numeric display in Text mode. It also supports Graphics mode and mixed display with Text. The supported maximum external display RAM is 64Kbyte and the display Window can be moved freely within the allocated memory range. The RA6963 has an 8-bit parallel data bus that can be directly connected to an 8080 series MCU.

The RA6963 supports a very broad range of LCD formats by allowing selection of different combinations via a set and combination text-and-graphic modes, and includes various attribute functions.

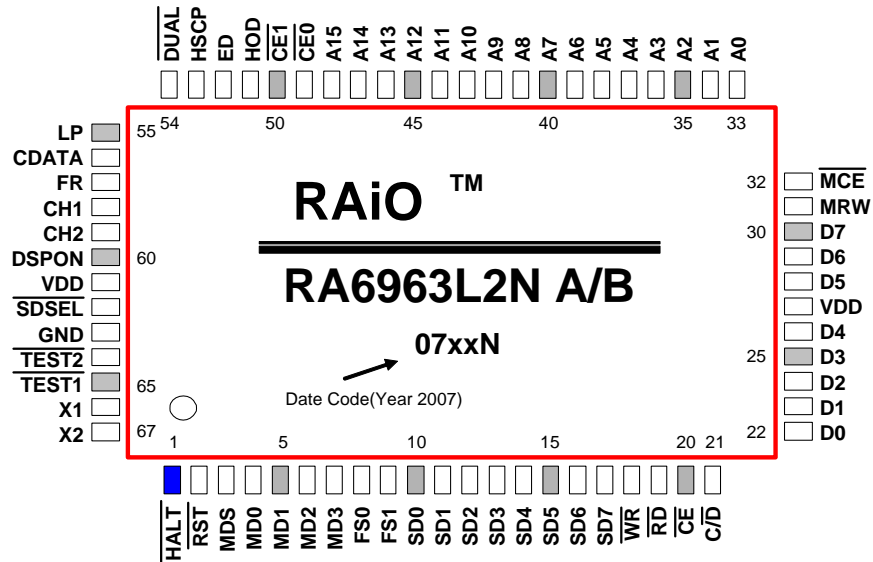
2. Features

- ◆ Support Display Range:
Columns → 32, 40, 64, 80
Rows → 2, 4, 6, 8, 10, 12, 14, 16, 20, 24, 28, 32
- ◆ Support 8080 8-bit MCU Interface
- ◆ Built-in 256-word Font ROM: Basic ASCII、Japanese、Numeric
- ◆ Support Max. 64Kbyte External Display SRAM
- ◆ Display Mode : Character、Graphics and Mixed Mode
- ◆ Font Size :
Horizontal → 5, 6, 7, 8 Pixels
Vertical → 8 Pixels
- ◆ Support Bold Font and Reverse Display
- ◆ Support Various LCD Driver
- ◆ Support 1/16 ~1/128 Duty
- ◆ Built-in X'tal Oscillator or Using External Clock
- ◆ Package: LQFP-67Pin (RoHS Compliance)

3. Block Diagram



4. Package



RA6963L2NA: LQFP-67 Pin, RoHS Compliance Package, Font-01
RA6963L2NB: LQFP-67 Pin, RoHS Compliance Package, Font-02
(Refer to Data Sheet Chapter 6-20)

5. Pin Descriptions

5.1 MCU Interface

Pin Name	I/O	Description									
SD[7..0]	I/O	Data Bus This is bus for data transfer between MCU and RA6963.									
\overline{RD}	I	Read Control \overline{RD} is a data read signal. When Low, MCU read data from RA6963.									
\overline{WR}	I	Write Control \overline{WR} is a data write signal. When Low, MCU write data into RA6963.									
C/ \overline{D}	I	Command/Data Select or Register Select This is a Data or Command select signal. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>C/\overline{D}</th> <th>\overline{WR} = Low</th> <th>\overline{RD} = Low</th> </tr> </thead> <tbody> <tr> <td>High</td> <td>Command Write</td> <td>Status Read</td> </tr> <tr> <td>Low</td> <td>Data Write</td> <td>Data Read</td> </tr> </tbody> </table>	C/ \overline{D}	\overline{WR} = Low	\overline{RD} = Low	High	Command Write	Status Read	Low	Data Write	Data Read
C/ \overline{D}	\overline{WR} = Low	\overline{RD} = Low									
High	Command Write	Status Read									
Low	Data Write	Data Read									
\overline{CS}	I	Chip Select This is chip enable of RA6963. When MCU communicate with RA6963, this pin must be Low.									

5.2 LCD Driver Interface

Pin Name	I/O	Description
FR	O	Frame
LP	O	Latch Latch pulse for column driver. Shift clock pulse for Row Driver
CDATA	O	Synchronous Data Synchronous Data for Row Driver.
HSCP	O	Shift Clock Pulse Shift clock pulse for Column Driver in upper area of LCD.
HOD	O	Data Output Data output for Odd Columns in upper area of LCD.
ED	O	Data Output $\overline{\text{SDSEL}} = \text{High} \rightarrow$ Data output for even columns in both upper and lower area of LCD. $\overline{\text{SDSEL}} = \text{Low} \rightarrow$ Data output for columns in both upper and lower area of LCD.
DSPON	O	Display On Display On/Off control signal. When $\overline{\text{HALT}}$ or $\overline{\text{RST}}$ is Low, DSPON output Low (LCD Display Off).

5.3 Memory Interface

Pin Name	I/O	Description
A[15:0]	O	Address Output for External Memory
D[7:0]	I/O	Data Bus for External Memory
$\overline{\text{MCE}}$	O	Memory Chip Enable $\overline{\text{MCE}} = \text{Low} \rightarrow$ Memory Enable. $\overline{\text{MCE}} = \text{High} \rightarrow$ Memory Disable.
MRW	O	Memory Read/Write Control MRW = Low \rightarrow Memory Write Enable. MRW = High \rightarrow Memory Read Enable.
$\overline{\text{CE0}}$ LOD	O	Memory Chip Enable 0 If $\overline{\text{DUAL}} = \text{High} \rightarrow$ Chip enable pin for display memory in the address range 0000~07FFh. If $\overline{\text{DUAL}} = \text{Low} \rightarrow$ Serial data output for odd columns in lower area of LCD.
$\overline{\text{CE1}}$ LSCP	O	Memory Chip Enable 1 If $\overline{\text{DUAL}} = \text{High} \rightarrow$ Chip enable pin for display memory in the address range 0800~0FFFh. If $\overline{\text{DUAL}} = \text{Low} \rightarrow$ Shift clock output for Column Driver in lower area of LCD.
VDD	P	Power
GND	P	Ground

5.4 Misc. Interface

Pin Name	I/O	Description																																																																																																												
$\overline{\text{DUAL}}$	I	Scan Select $\overline{\text{DUAL}}$ = Low → Dual-Scan Mode. $\overline{\text{DUAL}}$ = High → Signal-Scan Mode.																																																																																																												
MDS MD[1:0]	I	LCD Size Selection One Screen: <table border="1" style="margin-left: 20px;"> <tr><td>DUAL</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td><td>H</td></tr> <tr><td>MDS</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr> <tr><td>MD1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr> <tr><td>MD0</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr><td>Lines</td><td>2</td><td>4</td><td>6</td><td>8</td><td>10</td><td>12</td><td>14</td><td>16</td></tr> <tr><td>V-Dots</td><td>16</td><td>32</td><td>48</td><td>64</td><td>80</td><td>96</td><td>112</td><td>128</td></tr> </table> Two Screens: <table border="1" style="margin-left: 20px;"> <tr><td>DUAL</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td><td>L</td></tr> <tr><td>MDS</td><td>L</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td><td>H</td><td>H</td></tr> <tr><td>MD1</td><td>H</td><td>H</td><td>L</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr> <tr><td>MD0</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr><td>Lines</td><td>4</td><td>8</td><td>12</td><td>16</td><td>20</td><td>24</td><td>28</td><td>32</td></tr> <tr><td>V-Dots</td><td>32</td><td>64</td><td>96</td><td>128</td><td>160</td><td>192</td><td>224</td><td>256</td></tr> </table>	DUAL	H	H	H	H	H	H	H	H	MDS	L	L	L	L	H	H	H	H	MD1	H	H	L	L	H	H	L	L	MD0	H	L	H	L	H	L	H	L	Lines	2	4	6	8	10	12	14	16	V-Dots	16	32	48	64	80	96	112	128	DUAL	L	L	L	L	L	L	L	L	MDS	L	L	L	L	H	H	H	H	MD1	H	H	L	L	H	H	L	L	MD0	H	L	H	L	H	L	H	L	Lines	4	8	12	16	20	24	28	32	V-Dots	32	64	96	128	160	192	224	256
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X1	I	Crystal Oscillator Input A crystal / ceramic oscillator circuit is built in. The oscillation frequency is adjusted according to the display size. If using an external clock, use the X1 pin as the clock input. (X2 open.) External capacitors 15 to 20pF for Crystal or Ceramic oscillator.																																																																																																												
X2	O	Crystal Oscillator Output																																																																																																												
FS[1:0]	I	Font Selection <table border="1" style="margin-left: 20px;"> <tr><td>FS0</td><td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr><td>FS1</td><td>H</td><td>H</td><td>L</td><td>L</td></tr> <tr><td>Font</td><td>5 X 8</td><td>6 X 8</td><td>7 X 8</td><td>8 X 8</td></tr> </table>	FS0	H	L	H	L	FS1	H	H	L	L	Font	5 X 8	6 X 8	7 X 8	8 X 8																																																																																													
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MD[3:2]	I	Columns Selection <table border="1" style="margin-left: 20px;"> <tr><td>MD2</td><td>H</td><td>L</td><td>H</td><td>L</td></tr> <tr><td>MD3</td><td>H</td><td>H</td><td>L</td><td>L</td></tr> <tr><td>Columns</td><td>30</td><td>40</td><td>64</td><td>80</td></tr> </table>	MD2	H	L	H	L	MD3	H	H	L	L	Columns	30	40	64	80																																																																																													
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$\overline{\text{SDSEL}}$	I	Data Transfer Mode $\overline{\text{SDSEL}}$ = Low → Sending data by simple serial mode. $\overline{\text{SDSEL}}$ = High → Sending data by odd/even separation mode.																																																																																																												
$\overline{\text{HALT}}$	I	Halt Signal $\overline{\text{HALT}}$ = Low → Stop the Clock.																																																																																																												

		HALT = High → Normal Mode.
RST	I	Reset Signal RST = Low → RA6963 will be reset. RST = High → Normal mode. RA6963 built-in a Pull-Hi resistor.
TEST[2:1]	I	Test Pins These are test pins. No need for connection(NC).
CH1, CH2	O	Check Signals
FONTSEL	I	CGROM Font Select This pin is used to select the character of CGROM. Refer to Chapter 6-20. Please note, this pin is only reserved for die base chip only. Refer to complete specification Chapter 7-2. FONTSEL = Low → Select CGROM Font 01. FONTSEL = High → Select CGROM Font 02.

6. System Application

